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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,011	HEER, CHRISTOPH	
	Examiner	Art Unit	
	Peter Coughlan	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/9/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to an AMENDMENT entered April 28, 2006 for the patent application 10/724011 filed on November 26, 2003.

2. The First Office Action of February 1, 2006 is fully incorporated into this Final Office Action by reference.

Status of Claims

3. Claims 1-14 are pending.

Drawings

4. In the non-final office action the Examiner stated there were 6 inputs for the CLB control logic and the claims state there are only 4 inputs. Per the application the CLB control logic is item #8 in figure #1. The CLB control logic has 6 inputs, bus 17 from input node 10, bus 7 from input node 1, the output of register 3, the output of register 6, the output of register 16, and the output of register 13, totaling 6 inputs into the CLB control logic 8.

35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-10 and 14 are rejected under 35 U.S.C. 101 for nonstatutory subject matter. The computer system must set forth a practical application of that § 101 judicial exception to produce a real-world result. Benson, 409 U.S. at 71-72, 175 USPQ at 676-77. The invention is ineligible because it has not been limited to a substantial practical application. An arrangements of logic blocks or a logic circuit has no defined practical application. As stated in these claims the logic blocks or circuit could have a number of meanings. The result has to be a practical application. Please see the interim guidelines for examination of patent applications for patent subject matter eligibility published November 22, 2005 in the official gazette.

In determining whether the claim is for a "practical application," the focus is not on whether the steps taken to achieve a particular result are useful, tangible and concrete, but rather that the final result achieved by the claimed invention is "useful, tangible and concrete." If the claim is directed to a practical application of the § 101 judicial exception producing a result tied to the physical world that does not preempt the judicial exception, then the claim meets the statutory requirement of 35 U.S.C. § 101.

An arrangement of logic blocks that are arranged into a customer specific circuits has no defined limits, purpose, function, real world application, or practical application.

The invention must be for a practical application and either:

1) specify transforming (physical thing) or

2) have the FINAL RESULT (not the steps) achieve or produce a

useful (specific, substantial, AND credible),

concrete (substantially repeatable/ non-unpredictable), AND

tangible (real world/ non-abstract) result.

A claim that is so broad that it reads on both statutory and non-statutory subject matter, must be amended, and if the specification discloses a practical application but the claim is broader than the disclosure such that it does not require the practical application, then the claim must be amended.

Claims that describe a circuit design without a defined practical application and result are not statutory.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was

made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng in view of Mano and further in view of Barstow and further in view of Hellstrand and further in view of Miller. (U. S. Patent Publication 20020152060, referred to as **Tseng**; 'Logic and Computer Design Fundamentals', referred to as **Mano**; U. S. Patent 4827404, referred to as **Barstow;** U. S. Patent Publication 20020019969, referred to as **Hellestrand;** U. S. Patent 6181164, referred to as **Miller**)

Claim 1.

Tseng teaches an input data node for carrying input data (**Tseng**, ¶[0523]).

Tseng does not teach a CLB control logic circuit having a first input, a second input, a third input, a fourth input and an output.

Mano teaches teach a CLB control logic circuit having a first input, a second input, a third input, a fourth input and an output (**Mano**, Page 351, figure 7-5 (The components of the OR gate, the MUX and the load comprise the control logic circuit); The CLB control logic can be anything. This figure illustrates the four inputs being K1, K2, output of R2 and output for R1. There is a fifth input for the clock (See claim specification) The output is Q_0-Q_3 from R0.). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Tseng by having a control unit that uses current input to dictate the operations of the CLB as taught by Mano to have a CLB control logic circuit having a first input, a second input, a third input, a fourth input and an output.

For the purpose of the CLB to operate with current information.

Tseng and Mano do not teach at least one look-up table in which a switching function of at least one conditional branch is implemented with content addressability, wherein the at least one look-up table generates an "if then else" branch that realizes a comparison of the input data with comparison data previously stored in the at least one look-up table, and wherein a result output of the at least one look-up table is provided to the third input of the CLB control logic.

Barstow teaches at least one look-up table in which a switching function of at least one conditional branch is implemented with content addressability, wherein the at least one look-up table generates an "if then else" branch that realizes a comparison of the input data with comparison data previously stored in the at least one look-up table, and wherein a result output of the at least one look-up table is provided to the third input of the CLB control logic (**Barstow**, C12:36 through C13:2 and C14:65 through C15:17; In C12:36 through C13:2 Barstow illustrates the steps taken when going through the 'if' , 'then' and 'else' conditions. In order to make the changes between these steps is called a switch which Barstow illustrates in C14:65 through C15:17.). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Tseng and Mano by giving the details on how a look-up table work in finding a if-then-else statement as taught by Barstow to have at least one look-up table in which a switching function of at least one conditional branch is implemented with content addressability, wherein the at least one look-up table generates an "if then else" branch that realizes a comparison of the input data with

comparison data previously stored in the at least one look-up table, and wherein a result output of the at least one look-up table is provided to a third input of the CLB control logic.

For the purpose of having the ability to identify a if-then-else statement.

Tseng teaches an input data bus coupled between the input data node and a bus input of the at least one look-up table, wherein the first input of the CLB control logic circuit is coupled to the input data node via the input data bus(**Tseng**, ¶[0242]).

Tseng, Mano and Barstow do not teach at least one multiplexer having a control input coupled to the input data node and also to the first input of the CLB control logic circuit via at least part of the bit width of the input data bus, an output of the at least one multiplexer being coupled to the fourth input of the CLB control logic.

Hellestrand teaches at least one multiplexer having a control input coupled to the input data node and also to the first input of the CLB control logic circuit via at least part of the bit width of the input data bus, an output of the at least one multiplexer being coupled to the fourth input of the CLB control logic (**Hellestrand**, ¶[0310], ¶[0311] and figure 16; In figure 16, item 1609 is a multiplexer and 'asynch event control of Hellestrand is equivalent to 'logic circuit' of applicant.). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to combined teachings of Tseng, Mano and Barstow by having the control logic operate with current input data as taught by Hellestrand to have at least one multiplexer having a control input coupled to the input data node and also to the first input of the CLB control logic

circuit via at least part of the bit width of the input data bus, an output of the at least one multiplexer being coupled to a fourth input of the CLB control logic.

For the purpose of operating with current inputted data results in improved results.

A control input node coupled via a control bus to the second input of the CLB control logic (See Claim Rejections - 35 USC § 112).

Tseng, Mano, Barstow and Hellstrand do not teach at least one register data bus coupled between a register data bus output of the at least one look-up table and a bus input of the at least one multiplexer.

Miller teaches at least one register data bus coupled between a register data bus output of the at least one look-up table and a bus input of the at least one multiplexer (**Miller**, figure 4 and C5:47-51). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Tseng, Mano, Barstow and Hellstrand by illustrating the connections between the modules as taught by MIller to have at least one register data bus coupled between a register data bus output of the at least one look-up table and a bus input of the at least one multiplexer.

For the purpose of using the inputted data and comparing it with what is stored in the registers with the results of this look up table being sent to a multiplexer for a further decision to be made then.

Claim 2.

Tseng does not teach a register which stores the comparison data; and a comparator coupled to the input data node and the register, the comparator operable to compare the input data with the comparison data.

Mano teaches a register which stores the comparison data (**Mano**, page 352, figure 7-6(a); R0 would store the input data. R1 is equivalent to 4 in figure 1 of applicant. R2 is equivalent to 14 in figure 1 of applicant.); and a comparator coupled to the input data node and the register, the comparator operable to compare the input data with the comparison data. (**Mano**, page 29, table 2-1 (truth table for 'AND' page 30) page 31 (a) Graphic symbol for a 2 input AND gate; 'AND' is only one of many comparison models to use. To construct a comparator using only AND gates with n inputs, a total of n-1 and gates is needed. Let the 'X' input be connected to the register and the 'Y' input be connected to the input.). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Tseng by having known data stored in a register and using it to compare with incoming data as taught by Mano to store the comparison data; and a comparator coupled to the input data node and the register, the comparator operable to compare the input data with the comparison data.

For the purpose of having a working schematic diagram that fulfills the purpose of storing data and comparing it with incoming data.

Claims 4, 14.

Tseng does not teach the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology.

Mano teaches teach the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology (**Mano**, pages 330-334). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Tseng by using logic blocks that can be programmed as taught by Tseng to have the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology.

For the purpose of short development time, lower production costs, and favorable system modifications.

Claim 5.

Tseng does not teach the output of the CLB control logic serving as an output of the CLB.

Mano teaches the output of the CLB control logic serving as an output of the CLB (**Mano**, page 351 figure 7-5(b); The contents of this figure are sections (but not all inclusive) of the CLB and the 2-to-1 MUX, the OR gate with K1 and K2 as inputs for the OR gate, and R0 comprises the CLB control logic. One can see the 4 inputs K1, K2, R2(Q_{0-3}) and R1(Q_{0-3}) result in a single output R0(Q_{0-3})). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Tseng by designing the schematic so that the final result would be

outputted from the CLB control logic as taught by Mano to have output of the CLB control logic serving as an output of the CLB.

For the purpose of having a single output in the CLB.

Claim Rejections - 35 USC § 103

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tseng, Mano, Barstow Hellstrand and Miller, as set forth above, and further in view of Udagawa. (U. S. Patent 6388767, referred to as **Udagawa**)

Claim 3.

Tseng, Mano, Barstow Hellstrand and Miller do not teach the bus input of the at least one look-up table is coupled to a first bus input of the comparator and wherein a bus output of the register (4), (14) is coupled to a second bus input of the comparator and also to the register data bus output of the at least one look-up table, and wherein an output of the comparator is coupled to the result output of the at least one look-up table.

Udagawa teaches the bus input of the at least one look-up table is coupled to a first bus input of the comparator and wherein a bus output of the register (4), (14) is coupled to a second bus input of the comparator and also to the register data bus output of the at least one look-up table, and wherein an output of the comparator is coupled to the result output of the at least one look-up table (**Udagawa**, figure 4 and C9:47 through C10:8; Udagawa has these three modules set up te same way as applicant.). It would have been obvious to a person having ordinary skill in the art at the

time of applicant's invention to modify combined teachings of Tseng, Mano, Barstow Hellstrand and Miller by illustrating the connections between the look-up table, comparator and the register as taught by Udagawa to illustrate the bus input of the at least one look-up table is coupled to a first bus input of the comparator and wherein a bus output of the register (4), (14) is coupled to a second bus input of the comparator and also to the register data bus output of the at least one look-up table, and wherein an output of the comparator is coupled to the result output of the at least one look-up table.

For the purpose of having a schematic diagram that illustrates the connections between the look-up table, comparator and register.

Claim Rejections - 35 USC § 103

Claims 6, 7, 8, 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tseng, Mano, Barstow Hellstrand and Miller, as set forth above, and further in view of Nataraj. (U. S. Patent Publication 20020161969, referred to as **Nataraj**)

Claim 6.

Tseng does not teach a register; a comparator with a first input coupled to the register and with a second input coupled to an input node; a multiplexer with an input coupled to the register.

Mano teaches a register (**Mano**, page 352, figure 7-6(a); See claim 2); a comparator with a first input coupled to the register and with a second input coupled to an input node (**Mano**, page 29, table 2-1 (truth table for 'AND' page 30) page 31 (a)Graphic symbol for a 2 input AND gate; See Claim 2, the connection to the register is the 'X' input and the connection to the input node is the 'Y' input.); a multiplexer with an input coupled to the register (**Mano**, page 29, table 2-1 (truth table for 'AND' page 30) page 31 (a)Graphic symbol for a 2 input AND gate; See claim 2). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Tseng by connecting the components of a register, comparator, a multiplexer as taught by Mano to have a register; a comparator with a first input coupled to the register and with a second input coupled to an input node; a multiplexer with an input coupled to the register.

For the purpose of comparing input values to aid in the execution of the 'if-then-else' logic.

Tseng, Mano, Barstow Hellstrand and Miller do not teach a control block with inputs coupled to the multiplexer, the comparator, the input node and a control input node, wherein the logic circuit realizes an "if then else" branch based upon information carried at the input node and information stored in the register.

Nataraj teaches a control block with inputs coupled to the multiplexer (**Nataraj**, ¶[0043]), the comparator (**Nataraj**, ¶[0248]), the input node and a control input node (**Nataraj**, ¶[0155]), wherein the logic circuit realizes an "if then else" (**Nataraj**, ¶[0094]) branch based upon information carried at the input node and information stored in the

register. It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Mano by illustrating the relationships us multiplexers, inputs, comparators with CLB for realizing a if-then-else as taught by Nataraj to a control block with inputs coupled to the multiplexer, the comparator, the input node and an input control node, wherein the logic circuit realizes an "if then else" branch based upon information carried at the input node and information stored in the register.

For the purpose of illustrating the modules needed to have a if-then-else realized.

Claim 7.

Tseng does not teach logic circuit comprises a configurable logic block.

Mano teaches the logic circuit comprises a configurable logic block (**Mano**, page 351 figure 7-5(b) See claim 5. Register of applicant is equivalent to R0 of Mano. Comparator of applicant is equivalent to the OR gate of Mano. And the input node of applicant is equivalent to the 4 inputs K1, K2, R1(Q_{0-3}) and R2(Q_{0-3}) of Mano). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Tseng by illustrating a configurable logic block makes up the logic circuit as taught by Mano to have teach logic circuit comprises a configurable logic block.

For the purpose of illustrating the logic block construction into a logic circuit is of a standard design.

Claims 8.

Tseng does not teach the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology.

Mano teaches teach the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology (**Mano**, pages 330-334). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Tseng by using logic blocks that can be programmed as taught by Tseng to have the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology.

For the purpose of short development time, lower production costs, and favorable system modifications.

Claim 9.

Tseng does not teach a second register; a second comparator with a first input coupled to the second register and with a second input coupled to the input node.

Mano teaches a second register (**Mano**, page 352, figure 7-6(a); See claim 2); a second comparator with a first input coupled to the second register and with a second input coupled to the input node (**Mano**, page 352, figure 7-6(a) and page 29, table 2-1 (truth table for 'AND' page 30) page 31 (a) Graphic symbol for a 2 input AND gate; See claims 2 and 6); a second multiplexer with an input coupled to the second register (**Mano**, page 352, figure 7-6(a); See claim 2). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings

of Tseng by having the hardware to perform the 'then' function of the 'if-then-else' circuit as taught by to have a second register; a second comparator with a first input coupled to the second register and with a second input coupled to the input node.

For the purpose of executing a portion of the circuits design.

Tseng, Mano, Barstow Hellstrand and Miller do not teach the control block is coupled to the second comparator and the second multiplexer.

Nataraj teaches the control block is coupled to the second comparator and the second multiplexer (**Nataraj**, ¶[0248]). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Mano by having a second pair of comparator and multiplexer so further comparisons can be made as taught by Nataraj to have the control block is coupled to the second comparator and the second multiplexer.

For the purpose of having the expandable capabilities for future uses.

Claim 10.

Tseng does not teach the output of the CLB control logic serving as an output of the logic circuit.

Mano teaches the output of the CLB control logic serving as an output of the logic circuit. (**Mano**, page 351 figure 7-5(b); See claim 5) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Tseng by having the hardware to provide the 'then' portion or the 'else'

portion through a common port as taught by Mano to have the output of the CLB control logic serving as an output of the logic circuit.

For the purpose of the circuit providing the correct solution through a common node so it can be easily incorporated into a larger circuit without concerns which node the correct solution will be outputted.

Claim Rejections - 35 USC § 103

Claims 11, 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tseng, Mano, Barstow Hellstrand and Miller, as set forth above, and further in view of Nomura. (U. S. Patent 6317362, referred to as **Nomura**)

Claim 11.

Tseng and Mano do not teach means for performing a switching function of at least one conditional branch is implemented with content addressability, wherein the means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored comparison data; means, coupled to the means for performing a switch function, for selecting at least a portion of the comparison data; and a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting.

Barstow teaches means for performing a switching function of at least one conditional branch is implemented with content addressability, wherein the means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored comparison data (**Barstow**, C12:36 through C13:2); means, coupled to the means for performing a switch function, for selecting at least a portion of the comparison data (**Barstow**, C12:36 through C13:2 and C14:65 through C15:17; In C12:36 through C13:2 Barstow illustrates the steps taken when going through the 'if' , 'then' and 'else' conditions. In order to make the changes between these steps is called a switch which Barstow illustrates in C14:65 through C15:17.). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Tseng and Mano by having the ability to switch as needed for an 'if then else' branch as taught by Barstow to have the means for performing a switching function of at least one conditional branch is implemented with content addressability, wherein the means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored comparison data; means, coupled to the means for performing a switch function, for selecting at least a portion of the comparison data.

For the purpose of being able to switch after a select has been chosen. Tseng, Mano, Barstow Hellstrand and Miller a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting.

Nomura teaches a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting (**Nomura**, C8:9-10 and 45-55). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings Tseng, Mano, Barstow Hellstrand and Miller by having three inputs related to input data, selecting and switching as taught by Nomura to have a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting.

For the purpose of determining what stage the circuit is currently is in to make the next correct move.

Claim 12.

Tseng does not teach for storing the comparison data; and means for comparing the comparison data and the input data.

Mano teaches means for storing the comparison data (**Mano**, page 352, figure 7-6(a); See claim 2; Comparison data would be stored in R1 or R2.); and means for comparing the comparison data and the input data (**Mano**, page 29, table 2-1 (truth table for 'AND' page 30) page 31 (a) Graphic symbol for a 2 input AND gate; See claim 2). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Tseng by having registers for storing the

'if' and 'then' portions(instructions) as taught by Mano to store the comparison data; and means for comparing the comparison data and the input data.

For the purpose of containing the instructions for the 'if-then-else' circuit.

Claim 13.

Tseng does not teach a register that stores the comparison data; and a comparator coupled to the register and to an input data node that carries the input data.

Mano teaches a register that stores the comparison data (**Mano**, page 352, figure 7-6(a); See claim 2; Comparison data would be stored in R1 or R2.) ; and a comparator coupled to the register and to an input data node that carries the input data (**Mano**, page 29, table 2-1 (truth table for 'AND' page 30) page 31 (a) Graphic symbol for a 2 input AND gate; See claim 2). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Tseng by storing the incoming data as taught by Mano to have a register that stores the comparison data; and a comparator coupled to the register and to an input data node that carries the input data.

For the purpose of holding such information is required till the comparison can be completed.

Response to Arguments

7. Applicant's arguments filed on April 28, 2006 for claims 1-14 have been fully considered but are not persuasive.

8. In reference to the Applicant's argument:

Claims 1-14 are pending in this application. Claims 1 and 6 are amended berein. Neither of these claims has been narrowed in scope. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

The drawings have been objected to because, per claim 1, the CLB control logic is supposed to have four inputs and a single output but in the figure there are six inputs. Applicant respectfully submits that the drawings show one exemplary embodiment. The claims are in no way limited to this one embodiment.

The abstract has been objected to because of an issue with regard to the "if-then-else" branch. To avoid any unintentional confusion, reference to this element has been eliminated from the abstract.

Claim 1 has been objected to because the claim requires four inputs and one output for the CLB control logic circuit but the lone figure shows five [sic. six] inputs, the fifth input being a clock pulse. Applicant respectfully submits that claim 1 recites the invention that Applicant intends to claim. No correction of this claim is necessary. The claim is not limited to the particular embodiment illustrated in the figure.

Examiner's response:

The logic circuit that performs the 'if-then-else' function only needs the components diagramed in figure 1. If the invention described by the application performs some additional function other than the 'if-then-else' function then this is not declared in the applicants claims. First Office Action stands.

9. In reference to the Applicant's argument:

Claims I -I 4 were rejected under 35 U.S.C. § 101 for reciting nonstatutory subject matter. Applicant respectfully disagrees with this rejection. Claim 1, as an example, very clearly recites an arrangement that includes a number of structural elements including an input node, a CLB control logic circuit, a lookup table, an input data bus, a multiplexer, a control input node, and a register data bus. Reference to case law that refers to a "claimed process" has absolutely no bearing on the structure claims recited in the present application.

Claims 3, 6, 9 and 1 I were rejected under 35 U.S.C. § 101 for lack of functional description. In particular, the Office Action states that "connection between modules with no explanation serves no function." Applicant respectfully submits that this conclusion is not based in any law, certainly not the statutory subject matter law surrounding Section 101.

Examiner's response:

Claims 1-10 and 14 stand rejected under 35 U.S.C. § 101. See section 5 above.

10. In reference to the Applicant's argument:

Claim 6 is rejected under 35 U,S.C. § 112, first paragraph., as failing to comply with the enablement requirement. In particular, the Office Action states that the claim is not enabled because the phrase "input control node" is not defined in the specification. Applicant respectfully submits that one of ordinary skill in the art would be able to implement an input control node without undue experimentation. That being said, the claim has been amended to use the same (and synonymous) term used in the specification.

Examiner's response:

Examiner withdraws the 35 U,S.C. § 112, first paragraph rejection.

11. In reference to the Applicant's argument:

Claims 1-14 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Tseng (U.S. Patent Publication No. 2002/0152060) in view of Mano ("Logic and

Computer Design Fundamentals," 2nd° Edition Updated), and further in view of Barstow (U.S. Patent No. 4,827,404), and further in view of Hellestrand (U.S. Patent Publication No. 200210019969), and further in view of Miller (U.S. Patent No. 6,181,164), and further in view of Udagawa {U.S. Patent No. 6,388,767), and further in view of Nataraj (U.S. Patent Publication No. 2002/0161969), and further in view of Nomura (U.S. Patent No. 6,317,362).

While Applicant understands that there is no limit to the number of references that can be used in a valid Section 103 rejection, Applicant points out that no fewer than five references have been relied upon to show the seven elements of claim 1. Of significant importance, none of these references provide any teaching or suggestion that they can be combined. In particular, the Office Action relies upon:

Tseng, which describes a XC4000 series FPGA;
Mario, at textbook that shows multiplexers used to select registers;

Bertow, which describes software to implement an if-then function;

Hellestand, which shows a virtual processor, and
Miller, which describes a programmable gate array.

Applicant respectfully submits that combination of these references is improper in order to obtain the present invention.. A Section. 103 rejection cannot be sustained by simply finding each of the elements in different, unrelated references. "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claim invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." MPEP §2143.01. In this case, no teaching, suggestion or motivation exists.

It is black letter law to state that Applicant is entitled to a patent unless prior art is found to anticipate or make obvious the claimed invention. 35 U.S.C. § 102. In other words, the Office holds the burden of proof in making a prior art rejection. In order to make such a rejection, the Office has the obligation to make a prima facie case of obviousness.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Examiner's response:

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is not what individual references themselves suggest but rather what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re Keller, 648 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983); In re McLaughlin, 170 USPQ 209 (CCPA 1971). References are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA 1969).

Examination Considerations

12. The claims and only the claims form the metes and bounds of the invention. "Office personnel are to give the claims their broadest reasonable interpretation in light of the supporting disclosure. *In re Morris*, 127 F.3d 1048, 1054-55, 44USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d, 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)" (MPEP p 2100-8, c 2, l 45-48; p 2100-9, c 1, l 1-4). The Examiner has the full latitude to interpret each claim in the broadest reasonable sense. Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

13. Examiner's Notes are provided to assist the applicant to better understand the nature of the prior art, application of such prior art and, as appropriate, to further indicate other prior art that maybe applied in other office actions. Such comments are entirely consistent with the intent and sprit of compact prosecution. However, and unless otherwise stated, the Examiner's Notes are not prior art but link to prior art that one of ordinary skill in the art would find inherently appropriate.

14. Examiner's Opinion: Paragraphs 12 and 13 apply. The Examiner has full latitude to interpret each claim in the broadest reasonable sense.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Claims 1-14 are rejected.

Correspondence Information

17. Any inquiry concerning this information or related to the subject disclosure should be directed to the Examiner Peter Coughlan, whose telephone number is (571) 272-5990. The Examiner can be reached on Monday through Friday from 7:15 a.m. to 3:45 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor David Vincent can be reached at (571) 272-3687. Any response to this office action should be mailed to:

Commissioner of Patents and Trademarks,

Washington, D. C. 20231;

Hand delivered to:

Receptionist,

Customer Service Window,

Randolph Building,

401 Dulany Street,

Alexandria, Virginia 22313,

(located on the first floor of the south side of the Randolph Building);

or faxed to:

(571) 273-8300 (for formal communications intended for entry.)

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Peter Coughlan

6/10/2006